WHAT IS CLAIMED IS:

1. A passive element chip comprising:

a substrate;

a plurality of passive elements formed on the substrate by metal wires; and

electrodes for electrically connecting the plurality of passive elements to an external source,

wherein the passive elements are isolated from each other.

2. The passive element chip according to Claim 1, wherein the plurality of passive elements is formed in an array.

3. The passive element chip according to Claim 1, wherein the plurality of passive elements includes one or a plurality of types of resistors, inductors and capacitors.

4. The passive element chip according to Claim 1, wherein the plurality of passive elements includes passive elements of a plurality of specifications.

5. The passive element chip according to Claim 4, wherein the specifications include a resistance value, a capacitance value, an inductance value, and a quality factor value.

6. The passive element chip according to Claim 1, wherein the plurality of passive elements is divided into a plurality of groups having mutually different specifications.

7. The passive element chip according to Claim 6, wherein the plurality of groups includes a group of high-frequency specifications and a group of low-frequency specifications.

8. The passive element chip according to Claim 6, wherein the groups include a group composed only of inductors, a group composed only of capacitors, or a group composed only of resistors.

9. The passive element chip according to Claim 1, wherein the plurality of passive elements includes only passive elements of high-frequency specifications or only passive elements of low-frequency specifications.

10. The passive element chip according to Claim 1, wherein the plurality of passive elements is composed only of inductors or capacitors.

11. The passive element chip according to Claim 1, wherein the passive elements are inductors formed of the metal wires spirally disposed.

12. The passive element chip according to Claim 1, wherein the passive elements are capacitors in which the metal wires constitute parallel plane electrodes.

13. The passive element chip according to Claim 1, further comprising:

an insulating layer covering the plurality of passive elements; and

a protective film that is deposited on the insulting layer and has openings,

wherein the electrodes have first electrodes that are formed on the insulating layer by being connected to the plurality of passive elements and exposed through the openings in the protective film.

14. The passive element chip according to Claim 12, wherein

the electrodes further have second electrodes electrically connected to the first electrodes, and

the second electrodes are covered with a resin layer expect for a part thereof.

15. A passive element chip formed by being diced off from a wafer, comprising:

a substrate;

a plurality of passive elements formed by metal

wires on the substrate; and

electrodes for electrically connecting the plurality of passive elements to an external source.

16. A highly integrated module comprising:

a passive element chip having a substrate, a plurality of passive elements formed by first metal wires on the substrate, and electrodes for electrically connecting the plurality of passive elements to an external source;

an active element chip having active elements and electrodes for electrically connecting the active elements to an external source; and

an insulating layer covering a plurality of the passive element chips and active element chip,

wherein the electrodes of the plurality of passive element chips and the electrodes of the plurality of active element chips are selectively connected by second metal wires.

17. A manufacturing method for a passive element chip having a plurality of passive elements, comprising:

a step for processing an insulating layer and metal wires and depositing them on a substrate to form a plurality of passive elements;

a step for forming, on the insulating layer, a plurality of first electrodes to be connected to the

plurality of passive elements; and

a step for covering the insulating layer with a protective film such that the plurality of first electrodes is exposed.

18. The manufacturing method for a passive element chip according to Claim 17, further comprising:

a step for covering the protective film with a photosensitive resin film such that the plurality of first electrodes is exposed;

a step for forming, on the photosensitive resin film, metal wires to be electrically connected to the plurality of first electrodes;

a step for forming second electrodes to be electrically connected to the metal wires; and

a step for covering the metal wires and the photosensitive resin film with a resin layer such that the second electrodes are partly exposed.

19. A manufacturing method for a highly integrated module having a plurality of insulating layers, comprising:

a step for disposing a passive element chip, which includes a substrate, a plurality of passive elements formed on the substrate by first metal wires, and electrodes for electrically connecting the plurality of passive elements to an external source, on a surface of one

of the plurality of insulating layers;

a step for disposing an active element chip, which has active elements and electrodes for electrically connecting the active elements to an external source, on a surface of one of the plurality of insulating layers; and

a step for electrically connecting the electrodes of the passive element chip and the electrodes of the active element chip by second metal wires.